AMENDMENT TO THE CLAIMS:

This listing of the claims replaces all prior versions, and listings, of claims in the application. Claims 18 and 19 are added.

1. (Original) A host platform/PVDM (packet voice data module) interface where the packet module includes at least one on-board DSP compatible with one particular host parallel bus protocol of a set of parallel bus protocols, said interface comprising:

a parallel bus coupled to the host ports of the DSP;

a non-volatile memory holding information indicating which one of the parallel bus protocols is utilized by the on-board DSP;

a serial bus coupled to the non-volatile memory for reading the information held on the non-volatile memory; and

termination logic, capable of implementing each protocol in the set of parallel bus protocols, for reading the information from the non-volatile memory and implementing the parallel bus protocol, identified by the non-volatile memory, utilized by the on-board DSP.

2. (Original) The interface of claim 1 further comprising:

a test and emulation bus for allowing diagnostic testing of on-board components.

3. (Original) The interface of claim 2 further comprising:

multiple time-division multiplexed buses coupled to the on-board DSP.

4. (Original) The interface of claim 1 where the PVDM includes a plurality of on-board DSPs, the interface further comprising:

a like plurality of DSP chip selects for selecting a particular one of the plurality of on-board DSPs to respond to the parallel bus; and

a hardware chip select for communication with a device on board the PVDM that provides special functionality.

5. (Original) The interface of claim 1 with said non-volatile memory further holding digital signature information utilized by the host for unambiguous module identification.

6. (Original) A method for interfacing a host platform and a PVDM (packet voice data module), where the packet module includes at least one on-board DSP (digital signal processor), which is compatible with one particular host parallel bus protocol out of a set of parallel bus protocols that can be implemented by host platform, and where the PVDM includes a non-volatile memory holding identification information identifying the type of on-board DSP, said method, with a configurable parallel bus and serial bus coupling the host platform and PVDM, said method, performed by host processor on the host platform, comprising the steps of:

reading the non-volatile memory over the serial bus to access the identification information to identify a particular parallel bus protocol, out of the set of parallel bus protocols, that is compatible with the on-board DSP; and

configuring the parallel bus to implement the particular parallel bus protocol to communicate with the on-board DSP.

7. (Original) The method of claim 6, where the non-volatile memory holds digital signature information, and further comprising the step of:

reading the digital signature information; and

unambiguously identifying the PVDM based on the digital signature information.

8. (Original) The method of claim 6 where a dedicated hardware chip select line couples the host platform to the PVDM and where the PVDM includes a non-DSP module, said method further comprising the step of:

utilizing the hardware chip select line to select the non-DSP module without disturbing DSP chip selecting functionality.

9. (Original) The method of claim 6 where said step of configuring the parallel bus further comprises the steps of:

selecting the function of a particular DMA control line of the bus to be compatible with the DMA operation of an identified on-board DSP.

10. (Original) A system for interfacing a host platform and a PVDM (packet voice data module), where the packet module includes at least one on-board DSP (digital signal processor), which is compatible with one particular host parallel bus protocol out of a set of parallel bus protocols that can be implemented by host platform, and where the PVDM includes a non-volatile memory holding identification information identifying the type of on-board DSP, with a configurable parallel bus and serial bus coupling the host platform and PVDM, said system comprising:

means for reading the non-volatile memory over the serial bus to access the identification information to identify a particular parallel bus protocol, out of the set of parallel bus protocols, that is compatible with the on-board DSP; and

means for configuring the parallel bus to implement the particular parallel bus protocol to communicate with the on-board DSP.

11. (Original) The system of claim 10, where the non-volatile memory holds digital signature information, and further comprising:

means for reading the digital signature information; and

means for unambiguously identifying the PVDM based on the digital signature information.

12. (Original) The system of claim 10 where a dedicated hardware chip select line couples the host platform to the PVDM and where the PVDM includes a non-DSP module, said system further comprising:

means for utilizing the hardware chip select line to select the non-DSP module without disturbing DSP chip selecting functionality.

13. (Original) The system of claim 10 where said means for configuring the parallel bus further comprises:

means for selecting the function of a particular DMA control line of the bus to be compatible with the DMA operation of an identified on-board DSP.

14. (Original) A computer program product, executed by a host processor, for interfacing a host platform and a PVDM (packet voice data module), where the packet module includes at least one on-board DSP (digital signal processor), which is compatible with one particular host parallel bus protocol out of a set of parallel bus protocols that can be implemented by host platform, and where the PVDM includes a non-volatile memory holding identification information identifying the type of on-board DSP, with a configurable parallel bus and serial bus coupling the host platform and PVDM, said computer program product comprising:

a computer usable medium having computer readable program code physically embodied therein, said computer program product further comprising:

computer readable program code executed by the host processor for reading the non-volatile memory over the serial bus to access the identification information to identify a particular parallel bus protocol, out of the set of parallel bus protocols, that is compatible with the on-board DSP; and

computer readable program code executed by the host processor for configuring the parallel bus to implement the particular parallel bus protocol to communicate with the on-board DSP.

15. (Original) The computer program product of claim 14, where the non-volatile memory holds digital signature information, and further comprising:

computer readable program code executed by the host processor for reading the digital signature information; and

computer readable program code executed by the host processor for unambiguously identifying the PVDM based on the digital signature information.

16. (Original) The computer program product of claim 14 where a dedicated hardware chip select line couples the host platform to the PVDM and where the PVDM includes a non-DSP module, said system further comprising:

computer readable program code executed by the host processor for utilizing the hardware chip select line to select the non-DSP module without disturbing DSP chip selecting functionality.

17. (Original) The computer program product of claim 14 where said means for configuring the parallel bus further comprises:

computer readable program code executed by the host processor for selecting the function of a particular DMA control line of the bus to be compatible with the DMA operation of an identified on-board DSP.

18. (New) A PVDM (packet voice data module) to be coupled to a slot on a motherboard, where the PVDM includes at least one on-board DSP compatible with one particular host parallel bus protocol of a set of parallel bus protocols, said PVDM comprising:

a parallel bus interface coupled to the host ports of the DSP, with the parallel bus interface adpated to be coupled to a parallel bus on the motherboard;

a non-volatile memory holding information indicating which one of the parallel bus protocols is utilized by the on-board DSP;

a serial bus interface coupled to the non-volatile memory to allow a processor on the motherboard to read the information held on the non-volatile memory so that termination logic on the motherboard, capable of implementing each protocol in the set of parallel bus protocols, can read the information from the non-volatile memory and implement the parallel bus protocol, identified by the non-volatile memory, utilized by the on-board DSP.

19. (New) A host platform having a motherboard including a processor and a slot for accepting a PVDM (packet voice data module) to be coupled to a slot on a motherboard, where the PVDM includes at least one on-board DSP compatible with one particular host parallel bus protocol of a set of parallel bus protocols and also includes a non-

volatile memory holding information indicating which one of the parallel bus protocols is utilized by the on-board DSP, said host platform comprising:

a parallel bus coupled to the host ports of the DSP, with the parallel bus interface adpated to be coupled to a parallel bus on the motherboard;

a serial bus interface adapted to be coupled to the non-volatile memory on the PVDM to allow the processor on the motherboard to read the information held on the non-volatile memory so that termination logic on the motherboard, capable of implementing each protocol in the set of parallel bus protocols, can read the information from the non-volatile memory and implement the parallel bus protocol, identified by the non-volatile memory, utilized by the on-board DSP.